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NEW APPLICATION TRANSMITTAL

Transmitted herewith for filing is the patent application of Inventor: Bruce A. Fairman

PROGRAMMABLE FIRST-IN FIRST-OUT (FIFO) MEMORY BUFFER FOR CONCURRENT DATA STREAM HANDLING

CERTIFICATION UNDER 37 CFR § 1.10

I hereby certify that this New Application and the documents referred to as enclosed herein are being deposited with the United States Postal Service on this date, November 6, 2000, in an envelope bearing "Express Mail Post Office To Addressee" Mailing Label Number EL703161567US addressed to: **PATENT APPLICATION**, Assistant Commissioner for Patents, Washington, D.C. 20231.

Tadas Narauskas
(Name of Person Mailing Paper)

Tadas Narauskas
Signature

Enclosed are:

1. The papers required for filing date under CFR § 1.53(b):

   19 Pages of Specification (including claims); 7 Sheet(s) of Drawings.
   X Formal
   — Informal

2. X Declaration or Oath (combined with Power of Attorney)
3. X Power of Attorney (combined with Declaration)
4. X Assignment of the Invention to Sony Corporation and Sony Electronics, Inc. (including Form PTO-1595).
5. Fee Calculation

   — Amendment changing number of claims or deleting multiple dependencies is enclosed.

CLAIMS AS FILED

	Number Filed	Number Extra	Rate	Basic Fee
				$710.00
Total Claims	46 - 20 =	26	$18.00	468.00
Independent Claims	6 - 3 =	3	$80 00	240.00
Multiple Dependent claim(s), if any			$270.00	
			Filing Fee Calculation	$1,418.00

6. 50% Filing Fee Reduction (if applicable)

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8. Payment of Fees

   X Check in the amount of $1458.00 (the amount to cover the basic filing fee is $1418.00 and $40.00 is to cover the assignment recordation fee) enclosed.

9. X Authorization to Charge Additional Fees

   The Commissioner is hereby authorized to charge any additional fees (or credit any overpayment) associated with this communication and which may be required under 37 CFR § 1.16 or § 1.17 to Account No. 08-1275. **An originally executed duplicate of this transmittal is enclosed for this purpose.**

10. — Information Disclosure Statement

11. X Return Receipt Postcard

Dated: November 6, 2000

By: Jonathan O. Owens
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Registration No.: 37,902

PATENT
SONY-14500

PROGRAMMABLE FIRST-IN FIRST-OUT (FIFO) MEMORY BUFFER FOR CONCURRENT DATA STREAM HANDLING

FIELD OF THE INVENTION:

The present invention relates to the field of receiving, storing and transmitting data. More particularly, the present invention relates to the field of managing and manipulating buffered data.

BACKGROUND OF THE INVENTION:

The IEEE standard, "IEEE 1394-2000 Standard For A High Performance Serial Bus," Draft ratified in 2000, is an international standard for implementing an inexpensive high-speed serial bus architecture which supports both asynchronous and isochronous format data transfers. Isochronous data transfers are real-time transfers which take place such that the time intervals between significant instances have the same duration at both the transmitting and receiving applications. Each packet of data transferred isochronously is transferred in its own time period. The IEEE 1394-2000 standard bus architecture provides up to sixty-four (64) channels for isochronous data transfer between applications. A six bit channel number is broadcast with the data to ensure reception by the appropriate application. This allows multiple applications to simultaneously transmit isochronous data across the bus structure. Asynchronous transfers are traditional data transfer operations which take place as soon as possible and transfer an amount of data from a source to a destination.

The IEEE 1394-2000 standard provides a high-speed serial bus for interconnecting digital devices thereby providing a universal I/O connection. The IEEE 1394-2000 standard defines a digital interface for the applications thereby eliminating the need for an application to convert digital data to analog data before it is transmitted across the bus. Correspondingly, a receiving application will receive digital data from the bus, not analog data, and will therefore not be required to convert analog data to digital data. The cable required by the IEEE 1394-2000 standard is very thin in size compared to other bulkier cables used to connect such devices. Devices can be added and removed from an IEEE 1394-2000 bus while the bus is active. If a device is so added or removed the bus will then automatically reconfigure itself for transmitting data between the then existing nodes. A node is considered a logical entity with a unique identification number on the bus structure. Each node provides an identification ROM, a standardized set of control registers and its own address space.

The IEEE 1394-2000 standard defines a protocol as illustrated in Figure 1. This protocol includes a serial bus management block 10 coupled to a transaction layer 12, a link layer 14 and a physical layer 16. The physical layer 16 provides the electrical and mechanical connection between a device or application and the IEEE 1394-2000 cable. The physical layer 16 also provides arbitration to ensure that all devices coupled to the IEEE 1394-2000 bus have access to the bus as well as actual data transmission and reception. The link layer 14 provides data packet delivery service for both asynchronous and isochronous data packet transport. This supports both asynchronous data transport, using an acknowledgement protocol, and isochronous data transport, providing real-time guaranteed bandwidth protocol for just-in-time data delivery. The transaction layer 12 supports the commands necessary to complete asynchronous data transfers, including read, write and lock. The serial bus management block 10 contains an isochronous resource manager for managing isochronous data transfers. The serial bus management block 10 also provides overall configuration control of the serial bus in the form of optimizing arbitration timing, guarantee of adequate electrical power for all devices on the bus, assignment of the cycle master, assignment of isochronous channel and bandwidth resources and basic notification of errors.

As discussed above, an IEEE 1394-2000 device includes the capability to transmit and receive data. This data can be of many different formats. Often data received by an IEEE 1394-2000 device must be processed. This processing includes any or all of displaying, manipulating, forwarding and storing. This processing can be performed in software controlled by the receiving application or in hardware. An example of an isochronous data pipe apparatus for processing received isochronous data, is taught within U.S. Patent Application Serial Number 08/612,322, filed on March 7, 1996 and entitled "ISOCHRONOUS DATA PIPE FOR MANAGING AND MANIPULATING A HIGH-SPEED STREAM OF ISOCHRONOUS DATA FLOWING BETWEEN AN APPLICATION AND A BUS STRUCTURE," which is hereby incorporated by reference.

First-in first-out (FIFO) buffers or memories are typically used as intermediate buffers during a data transfer where a buffer is needed and the order of the data, as received, must be maintained. FIFO's are generally implemented within a random access memory structure. A write pointer is used to keep track of the available memory locations. A read pointer is used to keep track of the occupied memory locations. As data is written to and read from the FIFO buffer, the write and read pointers are incremented, respectively, in order to maintain the order of the data so that the data is output from the FIFO buffer in the same order that it was received.

Typically, a FIFO only includes the ability to buffer the data by receiving the data, storing the data, and then providing the data at an output in the same order that the data was received.

SUMMARY OF THE INVENTION:

A programmable FIFO receives a stream of data to be buffered within the FIFO and then output from the FIFO. The programmable FIFO includes the ability to receive program instructions from an application or control circuit to perform specific operations on the stream of data before the data is provided as an output from the programmable FIFO. By performing the specific operations of the program instructions, the programmable FIFO has the ability to filter the stream of data as it passes through the FIFO, including re-ordering data within the FIFO, if appropriate, and also to synchronize the input and output of the stream of data with external input and output signals, respectively. The programmable FIFO also has the ability to operate as a typical FIFO and buffer the data without manipulating it. The programmable FIFO includes a programmable element and a FIFO memory and control circuit. The stream of data is stored within the FIFO memory and control circuit and then output in the appropriate order, depending on the program instructions. The programmable element includes a program memory in which the program instructions are stored and an execution unit which executes and performs the specific operations on the stream of data. Preferably, the programmable FIFO is implemented within a device configured for coupling to an IEEE 1394-2000 serial bus network. Alternatively, the programmable FIFO is implemented as a separate dedicated device within the IEEE 1394-2000 serial bus network.

In one aspect of the present invention, a method of buffering data within a first-in first-out buffer comprises receiving a stream of data to be buffered within the first-in first-out buffer, storing the stream of data within the first-in first-out buffer thereby forming a stored stream of data, obtaining a series of program instructions specifying operations to be performed on the stored stream of data and generating an output stream of data by executing the series of program instructions and performing the operations on the stored stream of data. The program instructions are obtained from an application or a control circuit. The stream of data is received from a bus structure. The bus structure is preferably an IEEE 1394 bus structure. The method further comprises transmitting the output stream of data from a buffer interface. Generating an output stream includes synchronizing the output stream of data to a time reference. A time reference is the cycle time of an IEEE 1394 bus structure.

In another aspect of the present invention, a method of buffering data within a first-in

first-out buffer comprises receiving a stream of data to be buffered within the first-in first-out buffer, storing the stream of data within the first-in first-out buffer thereby forming a stored stream of data, obtaining a series of program instructions specifying operations to be performed in relation to the stored stream of data and generating an output stream of data by executing the series of program instructions and performing the operations in relation to the stored stream of data, including synchronizing the output stream of data to a time reference. The program instructions are obtained from an application or a control circuit. The stream of data is received from a bus structure. The bus structure is preferably an IEEE 1394 bus structure. The method further comprises transmitting the output stream of data from a buffer interface. Generating an output stream of data includes manipulating the stored stream of data to form the output stream of data. A time reference is the cycle time of an IEEE 1394 bus structure.

In yet another aspect of the present invention, an apparatus for buffering data within a first-in first-out buffer comprises means for receiving a stream of data to be buffered within the first-in first-out buffer, means for storing the stream of data within the first-in first-out buffer thereby forming a stored stream of data, means for obtaining a series of program instructions specifying operations to be performed on the stored stream of data and means for generating an output stream of data by executing the series of program instructions and performing the operations on the stored stream of data. The program instructions are obtained from an application or a control circuit. The means for receiving a stream of data is coupled to a bus structure to receive the stream of data. The bus structure is preferably an IEEE 1394 bus structure. The apparatus further comprises means for transmitting coupled to the means for generating for transmitting the output stream of data. The means for generating synchronizes the output stream of data to a time reference. A time reference is the cycle time of an IEEE 1394 bus structure.

In still yet another aspect of the present invention, a programmable first-in first-out buffer comprises an input interface circuit configured to receive a stream of data to be buffered within the first-in first-out buffer, a data memory coupled to the input interface circuit to store the stream of data, thereby forming a stored stream of data, a program memory configured to obtain and store a series of program instructions specifying operations to be performed on the stored stream of data and an execution unit coupled to the program memory and to the data memory to generate an output stream of data by executing the series of program instructions and perform the operations on the stored stream of data. The program instructions are obtained from an application or a control circuit. The input interface circuit is coupled to a bus structure to receive

the stream of data. The bus structure is preferably an IEEE 1394 bus structure. The programmable first-in first-out buffer further comprises an output interface circuit coupled to the execution circuit and the data memory and configured to transmit the output stream of data. The execution unit synchronizes the output stream of data to a time reference. A time reference is the cycle time of an IEEE 1394 bus structure.

In yet another aspect of the present invention, a system comprises a bus interface circuit configured to couple to a bus structure and receive a stream of data, a data memory coupled to the bus interface circuit to store the stream of data, thereby forming a stored stream of data, wherein the data memory stores and outputs the stored stream of data thereby forming an output stream of data, a program memory configured to obtain and store a series of program instructions specifying operations to be performed on the stored stream of data and an execution unit coupled to the program memory and to the data memory to generate an output stream of data by executing the series of program instructions and performing the operations on the stored stream of data. The program instructions are obtained from an application or a control circuit. The bus structure is preferably an IEEE 1394 bus structure. The system further comprises an output interface circuit coupled to the execution unit and the data memory and configured to transmit the output stream of data. The execution unit synchronizes the output stream of data to a time reference. A time reference is the cycle time of an IEEE 1394 bus structure.

In still yet another aspect of the present invention, a network of devices comprises a plurality of devices, a bus structure coupled between the plurality of devices to transmit data between the devices and a programmable first-in first-out buffer including an input interface circuit configured to receive a stream of data to be buffered within the first-in first-out buffer, a data memory coupled to the input interface circuit to store the stream of data, thereby forming a stored stream of data, a program memory configured to obtain and store a series of program instructions specifying operations to be performed on the stored stream of data and an execution unit coupled to the program memory and to the data memory to generate an output stream of data by executing the series of program instructions and perform the operations on the stored stream of data. The program instructions are obtained from an application or a control circuit. The bus structure is preferably an IEEE 1394 bus structure. The network of devices further comprises an output interface circuit coupled to the execution unit and the data memory and configured to transmit the output stream of data. The execution unit synchronizes the output stream of data to a time reference. A time reference is the cycle time of an IEEE 1394 bus structure.

BRIEF DESCRIPTION OF THE DRAWINGS:

Figure 1 illustrates a protocol of the IEEE 1394-2000 standard.

Figure 2 illustrates an exemplary IEEE 1394-2000 serial bus network including a computer system and a video camera.

Figure 3 illustrates a block diagram of the internal components of the computer system 20.

Figure 4 illustrates an exemplary IEEE 1394-2000 serial bus network including a programmable FIFO embodied within a separate dedicated device.

Figure 5 illustrates a block diagram schematic of the programmable FIFO of the preferred embodiment of the present invention.

Figure 6 illustrates a block diagram schematic of the programmable element within the FIFO of the preferred embodiment of the present invention.

Figure 7 illustrates an exemplary stream of data stored within the FIFO memory and control circuit of the programmable FIFO.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT:

A programmable FIFO according to the present invention buffers a stream of data such that the data is filtered and output in an order, as determined by program instructions. Preferably, the programmable FIFO is included within a device coupled in an IEEE 1394-2000 serial bus network with other devices. Alternatively, the programmable FIFO is implemented within a separate component coupled within the IEEE 1394-2000 serial bus network. The programmable FIFO includes the ability to receive program instructions to perform specific operations on the stream of data while the stream of data is stored within the programmable FIFO. The program instructions are received from an application or control circuit. An application as used herein will refer to either an application or a device driver.

The programmable FIFO includes a programmable element and a FIFO memory and control circuit. The stream of data is stored within the FIFO memory and control circuit. The programmable element includes a program memory in which the program instructions are stored. The programmable element also includes an execution unit which executes the program instructions and performs the specific operations on the stream of data. In this manner, by performing program instructions the programmable FIFO has the ability to filter and re-order the stream of data as it passes through the FIFO. The programmable FIFO also has the ability to synchronize the input and output of the stream of data with external input and output signals,

respectively.

An exemplary IEEE 1394-2000 serial bus network implementing the present invention and including a computer system and a video camera is illustrated in Figure 2. The computer system 20 includes an associated display 22 and is coupled to the video camera 24 by the IEEE 1394-2000 serial bus cable 26. Video data and associated data are sent between the video camera 24 and the computer system 20 over the IEEE 1394-2000 serial bus cable 26.

A block diagram of the internal components of the exemplary computer system 20 is illustrated in Figure 3. The computer system 20 includes a central processor unit (CPU) 44, a main memory 30, a video memory 46, a mass storage device 32 and an IEEE 1394-2000 interface circuit 28, all coupled together by a conventional bidirectional system bus 34. The interface circuit 28 includes the physical interface circuit 42 for sending and receiving communications on the IEEE 1394-2000 serial bus and the programmable FIFO 52 which is used to buffer, filter and modify, as necessary, streams of data received and transmitted through the physical interface circuit 42. The physical interface circuit 42 is coupled to the camera 24 over the IEEE 1394-2000 serial bus cable 26. The system bus 34 contains an address bus for addressing any portion of the memory 30 and 46. The system bus 34 also includes a data bus for transferring data between and among the CPU 44, the main memory 30, the video memory 46, the mass storage device 32 and the interface circuit 28.

The computer system 20 is also coupled to a number of peripheral input and output devices including the keyboard 38, the mouse 40 and the associated display 22. The keyboard 38 is coupled to the CPU 44 for allowing a user to input data and control commands into the computer system 20. A conventional mouse 40 is coupled to the keyboard 38 for manipulating graphic images on the display 22 as a cursor control device. As is well known in the art, the mouse 40 can alternatively be coupled directly to the computer 20 through a serial port.

A port of the video memory 46 is coupled to a video multiplex and shifter circuit 48, which in turn is coupled to a video amplifier 50. The video amplifier 50 drives the display 22. The video multiplex and shifter circuitry 48 and the video amplifier 50 convert pixel data stored in the video memory 46 to raster signals suitable for use by the display 22.

Preferably, the programmable FIFO is included within a device coupled within an IEEE 1394-2000 serial bus network with other audio and video devices, such as within the computer system 20. Alternatively, the programmable FIFO is implemented within a separate component coupled within the IEEE 1394-2000 serial bus network.

In an alternate embodiment of the present invention, as illustrated in Figure 4, the

programmable FIFO is embodied within a separate dedicated component coupled to the IEEE 1394-2000 serial bus. The programmable FIFO 23 is coupled to the computer system 20 by the IEEE 1394-2000 serial bus 25. In this embodiment, any data stream sent to the programmable FIFO 23 is received, stored, manipulated, as appropriate according to the programmed instructions, and then transmitted to the target device.

A block diagram schematic of the components within the programmable FIFO of the preferred embodiment of the present invention is illustrated in Figure 5. The programmable FIFO 52 includes a data input interface 100 through which data is received to be stored within the FIFO 52. The data input interface 100 is coupled to a demultiplexer 102 which demultiplexes the stream of data received by the data input interface 100. The demultiplexer 102 is coupled to provide data to the FIFO memory and control circuit 104 and to the programmable element 106. The programmable element 106 is also coupled to control the demultiplexer 102. Based on the control signal from the programmable element 106, the demultiplexer 102 either directs the incoming data to the programmable element 106 or to the FIFO memory and control circuit 104. The programmable element 106 includes the control access interface 111 through which program instructions are preferably received from a controlling application or control circuit. In this manner, the programmable element 106 can receive program instructions and control signals from a means external to the programmable FIFO 52 and the FIFO memory and control circuit 104 is loaded with data that is to be buffered by the programmable FIFO 52. The programmable element 106 is also coupled to receive and transmit event and control signals to applications or control circuits external to the programmable FIFO 52.

The programmable element 106 includes an address bus, a data bus and a control bus which are coupled to the FIFO memory and control circuit 104 and are used to address, examine and manipulate the data within the FIFO memory and control circuit 104. An output of the FIFO memory and control circuit 104 is coupled as an input to a multiplexer 108. An output of the programmable element 106 is also coupled as an input to the multiplexer 108. The programmable element 106 is also coupled to control the multiplexer 108. The multiplexer 108 multiplexes the data from the programmable element 106 and from the FIFO memory and control circuit 104 and provides the multiplexed output stream to an output data interface 110. The output data interface 110 then provides the multiplexed output stream from the multiplexer 108 as the output of the programmable FIFO 52.

The inclusion of the programmable element 106 within the programmable FIFO 52 provides a mechanism that has the properties of a FIFO, with the additional capability to adapt

the behavior of the FIFO based on external knowledge of the format of the data stream flowing through the FIFO. The programmable element 106 is capable of being programmed by means external to the programmable FIFO 52, such as an application or control circuit, preferably through the control access interface 111. In the exemplary computer system of Figure 3, the programmable element 106 could alternatively be programmed by the CPU 44. Once programmed, the programmable element 106 then has the capability to monitor the input to the FIFO, generate the output of the FIFO and signal synchronization events at both the input and the output of the programmable FIFO 52. Preferably, the data width of the data paths and storage of the programmable element 106 are compatible with the data width of the FIFO memory and control circuit 104, by either being as wide as the data width of the FIFO memory and control circuit 104 or by being a sub-multiple of the data width of the FIFO memory and control circuit 104. Alternatively, the data paths and storage of the programmable element 106 have any appropriate data width.

A block diagram schematic of the components within the programmable element 106 of the preferred embodiment of the present invention is illustrated in Figure 6. The programmable element 106 includes a FIFO data input 152 and an external input/output interface 150. The FIFO data input 152 is coupled to the output of the demultiplexer 102 to receive the data input to the demultiplexer 102, as appropriate. The external input/output interface 150 is coupled to receive and transmit event and control signals from and to applications or control circuits external to the programmable FIFO 52. Both the FIFO data input 152 and the external input/output interface 150 are coupled to an execution unit 158, which includes a FIFO bus interface 155 through which the programmable element 106 receives and transmits data from and to the FIFO memory and control circuit 104 on the address and data buses. The FIFO bus interface 155 also includes the control signal lines which are coupled to control the demultiplexer 102 and the multiplexer 108. The execution unit 158 includes a program memory 156 which is used to store the instructions and commands to be performed on the data stored within the FIFO memory and control circuit 104. The execution unit 158 performs the instructions and commands stored in the program memory 156 on the data stored within the FIFO memory and control circuit 104. The processing performed in the programmable element 106 is preferably a parallel process in relation to the FIFO data input 152 and the FIFO data output 162. The nature of the FIFO operation provides the synchronization function necessary for this parallel processing.

The execution unit 158 and the program memory 156 are both coupled to the control

access unit 154. The control access unit 154 controls the operation of both the execution unit 158 and the program memory 156. As discussed above, the programmable element 106 is programmed by an application or control circuit through the control access interface. The execution unit 158 is also coupled to a FIFO data output 162 and to an external input/output interface 160. The external input/output interface 160 is coupled to transmit event signals to applications or control circuits external to the programmable FIFO 52. The FIFO data output 162 is coupled to the input of the multiplexer 108 to transmit data to be output by the multiplexer 108, as appropriate.

As described above, the normal operation of a FIFO is to maintain the order of the data and provide a buffering function, such that the data is output in the same order that it was received. In the programmable FIFO 52 of the present invention, the programmable element 106 is included. The inclusion of the programmable element 106 within the programmable FIFO 52 adds the capability to perform a programmable set of instructions or commands on the data as it passes through the programmable FIFO 52. The instructions and commands are defined for the format of the data passing through the programmable FIFO 52. The programmable FIFO 52 of the present invention operates as a typical FIFO and buffers the data, without manipulation of the data, if no manipulation or synchronization program instructions are stored within the program memory 156 of the programmable FIFO 52. However, the programmable element 106, when programmed to manipulate or perform instructions related to the stream of data passing through the programmable FIFO 52, allows the programmable FIFO 52 to manipulate or otherwise adapt the data, as programmed, as the stream of data passes through the programmable FIFO 52 and/or synchronize the output of the stream of data to a time reference. As an example, the availability of the FIFO output can be synchronized with an external time reference by having the processing element examine a format dependent field contained within the data passing through the programmable FIFO 52. Utilizing the address bus and the data bus, the data stored within the FIFO memory and control circuit 104 can be addressably accessed and processed according to the programmed instructions. This processing can also include re-ordering the data within the FIFO memory and control circuit 104 before it is output.

The instructions and commands to be performed on the data within the FIFO 52 are provided from an external application or control circuit and preferably stored within the program memory 156 in the programmable element 106. Alternatively, the instructions and commands are stored within an accompanying read-only memory. The event signals are used to synchronize the operation of the programmable element 106 with external time bases or other events. The

programmable element 106 is preferably a RISC-like processor for general purpose use. Alternatively, the programmable element 106 is a programmable sequencer or a state machine with appropriate input and output support. The instruction set stored within the program memory 156 and executed by the execution unit 158 reflects the kind of processing tasks for which the processing element is needed based on the type of data passing through the programmable FIFO 52.

The programmable FIFO 52 of the present invention can be used to perform programs that require examining data in the stream stored in the programmable FIFO 52. As an example of the operation of the programmable FIFO 52, the output of the programmable FIFO 52 can be synchronized with external events or time. Within an IEEE 1394-2000 serial bus packet of data, the data includes a header describing the synchronization criteria, such as time referenced to the local time base. In this example, this header can be part of the data within the stream or may be an application specific format that is removed before the data is output from the FIFO. The time base to which the output is to be synchronized can be local to the environment but in need of synchronization with a global time base, such as the cycle time of the IEEE 1394-2000 serial bus.

An exemplary stream of data stored within the FIFO memory and control circuit 104 is illustrated in Figure 7. The FIFO contents illustrated in Figure 7 are an example of using an embedded header control structure to provide synchronization information to the program executed by the processing element. In this example, the program instructions to synchronize the contents of the FIFO to a time base, are programmed into the program memory 156 by an application or control circuit, as described above. The execution unit 158 then executes the program instructions on the contents of the FIFO memory and control circuit 104. In this exemplary process, the contents of the header are stripped from the FIFO before the data field contents are provided from the output interface 110 of the FIFO. The contents of the header include the information needed by the execution unit 158 to implement proper synchronization of the local time base and the global time base, as well as allowing the data field contents to be correctly modified. Accordingly, by using the separated header bit, the execution unit 158 has the ability to then synchronize the output of the data field contents through the output interface 110 onto the IEEE 1394-2000 serial bus.

Another exemplary use of the programmable FIFO 52 of the present invention involves examining the stream of data received at the input interface 100 and filtering out unwanted portions of the stream of data. This approach is used to implement a form of trick play, such as fast-forward or rewind, when the received stream of data is from a recorded stream of data.

As described above, the programmable FIFO 52 of the present invention has the ability to be programmed by an external application or control circuit to execute a series of program instructions and perform a series of operations on a stream of data being buffered within the programmable FIFO 52. The stream of data can be any type of data including isochronous or asynchronous data. The series of program instructions are stored within the program memory 156 and executed by the execution unit 158. Both the program memory 156 and the execution unit 158 are preferably implemented within the programmable element 106 within the programmable FIFO 52. The stream of data is preferably stored within the FIFO memory and control circuit 104 within the programmable FIFO 52.

Adding this programmability and intelligence to the programmable FIFO 52 provides a mechanism allowing concurrent processing and synchronization of the stream of data being buffered within the programmable FIFO 52. The programmable FIFO 52 has the ability to filter the stream of data as it passes through the FIFO and also to synchronize the stream of data with external and output signals.

The present invention has been described in terms of specific embodiments incorporating details to facilitate the understanding of principles of construction and operation of the invention. Such reference herein to specific embodiments and details thereof is not intended to limit the scope of the claims appended hereto. It will be apparent to those skilled in the art that modifications may be made in the embodiment chosen for illustration without departing from the spirit and scope of the invention. Specifically, it will be apparent to those skilled in the art that while the preferred embodiment of the present invention is used within an IEEE 1394-2000 serial bus structure, the present invention could also be implemented on any other appropriate bus structures.

CLAIMS

I Claim:

1. A method of buffering data within a first-in first-out buffer comprising:
   a. receiving a stream of data to be buffered within the first-in first-out buffer;
   b. storing the stream of data within the first-in first-out buffer thereby forming a stored stream of data;
   c. obtaining a series of program instructions specifying operations to be performed on the stored stream of data; and
   d. generating an output stream of data by executing the series of program instructions and performing the operations on the stored stream of data.

2. The method as claimed in claim 1 wherein the program instructions are obtained from an application.

3. The method as claimed in claim 1 wherein the program instructions are obtained from a control circuit.

4. The method as claimed in claim 1 wherein the stream of data is received from a bus structure.

5. The method as claimed in claim 4 wherein the bus structure is an IEEE 1394 bus structure.

6. The method as claimed in claim 1 further comprising transmitting the output stream of data from a buffer interface.

7. The method as claimed in claim 1 wherein generating an output stream includes synchronizing the output stream of data to a time reference.

8. The method as claimed in claim 7 wherein the time reference is a cycle time of an IEEE 1394 bus structure.

9. A method of buffering data within a first-in first-out buffer comprising:
   a. receiving a stream of data to be buffered within the first-in first-out buffer;
   b. storing the stream of data within the first-in first-out buffer thereby forming a stored stream of data;
   c. obtaining a series of program instructions specifying operations to be performed in relation to the stored stream of data; and
   d. generating an output stream of data by executing the series of program instructions and performing the operations in relation to the stored stream of data, including synchronizing the output stream of data to a time reference.

10. The method as claimed in claim 9 wherein the program instructions are obtained from an application.

11. The method as claimed in claim 9 wherein the program instructions are obtained from a control circuit.

12. The method as claimed in claim 9 wherein the stream of data is received from a bus structure.

13. The method as claimed in claim 12 wherein the bus structure is an IEEE 1394 bus structure.

14. The method as claimed in claim 9 further comprising transmitting the output stream of data from a buffer interface.

15. The method as claimed in claim 9 wherein generating an output stream of data includes manipulating the stored stream of data to form the output stream of data.

16. The method as claimed in claim 9 wherein the time reference is a cycle time of an IEEE 1394 bus structure.

17. An apparatus for buffering data within a first-in first-out buffer comprising:
   a. means for receiving a stream of data to be buffered within the first-in first-out

buffer;

b. means for storing the stream of data within the first-in first-out buffer thereby forming a stored stream of data;

c. means for obtaining a series of program instructions specifying operations to be performed on the stored stream of data; and

d. means for generating an output stream of data by executing the series of program instructions and performing the operations on the stored stream of data.

18. The apparatus as claimed in claim 17 wherein the program instructions are obtained from an application.

19. The apparatus as claimed in claim 17 wherein the program instructions are obtained from a control circuit.

20. The apparatus as claimed in claim 17 wherein the means for receiving a stream of data is coupled to a bus structure to receive the stream of data.

21. The apparatus as claimed in claim 20 wherein the bus structure is an IEEE 1394 bus structure.

22. The apparatus as claimed in claim 17 further comprising means for transmitting coupled to the means for generating for transmitting the output stream of data.

23. The apparatus as claimed in claim 17 wherein the means for generating synchronizes the output stream of data to a time reference.

24. The apparatus as claimed in claim 23 wherein the time reference is a cycle time of an IEEE 1394 bus structure.

25. A programmable first-in first-out buffer comprising:

a. an input interface circuit configured to receive a stream of data to be buffered within the first-in first-out buffer;

b. a data memory coupled to the input interface circuit to store the stream of data,

thereby forming a stored stream of data;

c. a program memory configured to obtain and store a series of program instructions specifying operations to be performed on the stored stream of data; and

d. an execution unit coupled to the program memory and to the data memory to generate an output stream of data by executing the series of program instructions and perform the operations on the stored stream of data.

26. The programmable first-in first-out buffer as claimed in claim 25 wherein the program instructions are obtained from an application.

27. The programmable first-in first-out buffer as claimed in claim 25 wherein the program instructions are obtained from a control circuit.

28. The programmable first-in first-out buffer as claimed in claim 25 wherein the input interface circuit is coupled to a bus structure to receive the stream of data.

29. The programmable first-in first-out buffer as claimed in claim 28 wherein the bus structure is an IEEE 1394 bus structure.

30. The programmable first-in first-out buffer as claimed in claim 25 further comprising an output interface circuit coupled to the execution circuit and the data memory and configured to transmit the output stream of data.

31. The programmable first-in first-out buffer as claimed in claim 25 wherein the execution unit synchronizes the output stream of data to a time reference.

32. The programmable first-in first-out buffer as claimed in claim 31 wherein the time reference is a cycle time of an IEEE 1394 bus structure.

33. A system comprising:

a. a bus interface circuit configured to couple to a bus structure and receive a stream of data;

b. a data memory coupled to the bus interface circuit to store the stream of data,

thereby forming a stored stream of data, wherein the data memory stores and outputs the stored stream of data, thereby forming an output stream of data;

c. a program memory configured to obtain and store a series of program instructions specifying operations to be performed on the stored stream of data; and

d. an execution unit coupled to the program memory and to the data memory to generate the output stream of data by executing the series of program instructions and performing the operations on the stored stream of data.

34. The system as claimed in claim 33 wherein the program instructions are obtained from an application.

35. The system as claimed in claim 33 wherein the program instructions are obtained from a control circuit.

36. The system as claimed in claim 33 wherein the bus structure is an IEEE 1394 bus structure.

37. The system as claimed in claim 33 further comprising an output interface circuit coupled to the execution unit and the data memory and configured to transmit the output stream of data.

38. The system as claimed in claim 33 wherein the execution unit synchronizes the output stream of data to a time reference.

39. The system as claimed in claim 38 wherein the time reference is a cycle time of an IEEE 1394 bus structure.

40. A network of devices comprising:

a. a plurality of devices;

b. a bus structure coupled between the plurality of devices to transmit data between the devices; and

c. a programmable first-in first-out buffer including:

i. an input interface circuit configured to receive a stream of data to be

buffered within the first-in first-out buffer;

ii. a data memory coupled to the input interface circuit to store the stream of data, thereby forming a stored stream of data;

iii. a program memory configured to obtain and store a series of program instructions specifying operations to be performed on the stored stream of data; and

iv. an execution unit coupled to the program memory and to the data memory to generate an output stream of data by executing the series of program instructions and perform the operations on the stored stream of data.

41. The network of devices as claimed in claim 40 wherein the program instructions are obtained from an application.

42. The network of devices as claimed in claim 40 wherein the program instructions are obtained from a control circuit.

43. The network of devices as claimed in claim 40 wherein the bus structure is an IEEE 1394 bus structure.

44. The network of devices as claimed in claim 40 further comprising an output interface circuit coupled to the execution unit and the data memory and configured to transmit the output stream of data.

45. The network of devices as claimed in claim 40 wherein the execution unit synchronizes the output stream of data to a time reference.

46. The network of devices as claimed in claim 45 wherein the time reference is a cycle time of an IEEE 1394 bus structure.

ABSTRACT

A programmable FIFO receives a stream of data to be buffered within the FIFO and then output from the FIFO. The programmable FIFO includes the ability to receive program instructions from an application or control circuit to perform specific operations on the stream of data before the data is provided as an output from the programmable FIFO. By performing the specific operations of the program instructions, the programmable FIFO has the ability to filter the stream of data as it passes through the FIFO, including re-ordering data within the FIFO, if appropriate, and also to synchronize the input and output of the stream of data with external input and output signals, respectively. The programmable FIFO also has the ability to operate as a typical FIFO and buffer the data without manipulating it. The programmable FIFO includes a programmable element and a FIFO memory and control circuit. The stream of data is stored within the FIFO memory and control circuit and then output in the appropriate order, depending on the program instructions. The programmable element includes a program memory in which the program instructions are stored and an execution unit which executes and performs the specific operations on the stream of data. Preferably, the programmable FIFO is implemented within a device configured for coupling to an IEEE 1394-2000 serial bus network. Alternatively, the programmable FIFO is implemented as a separate dedicated device within the IEEE 1394-2000 serial bus network.

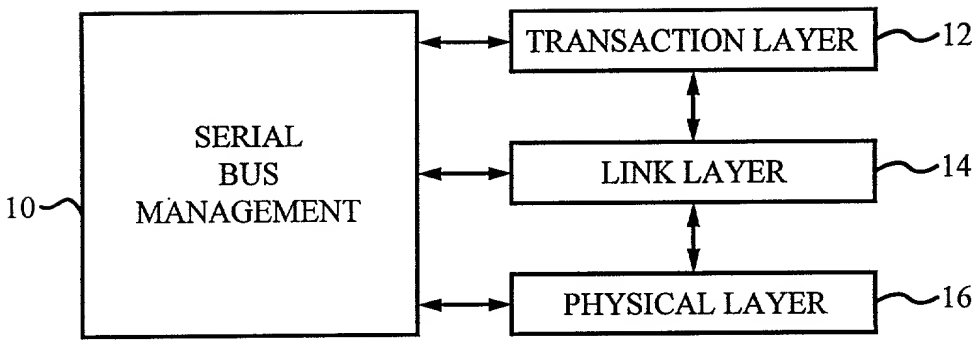


Fig. 1 (PRIOR ART)

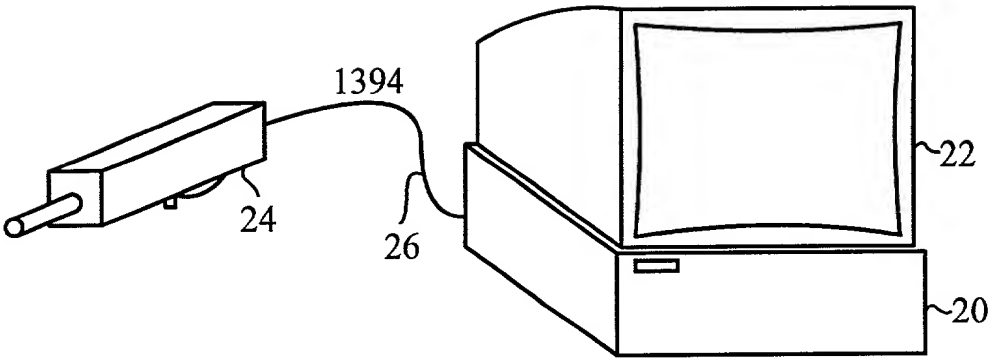
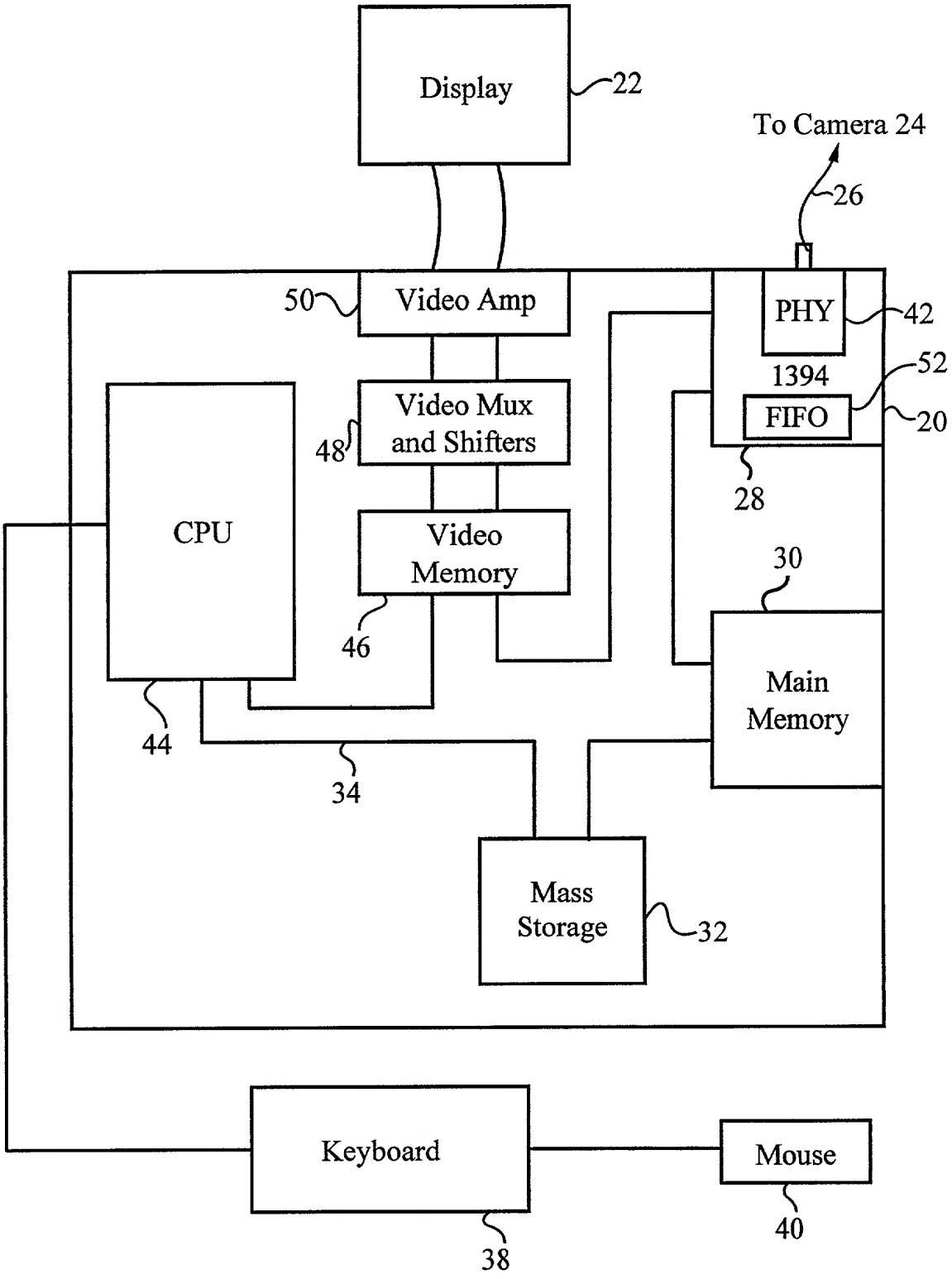


Fig. 2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To Camera 24
26
50
Video Amp
PHY
42
1394
52
FIFO
20
28
48
Video Mux
and Shifters
CPU
Video
Memory
46
30
Main
Memory
44
34
Mass
Storage
32
Keyboard
Mouse
38
40

Fig. 3

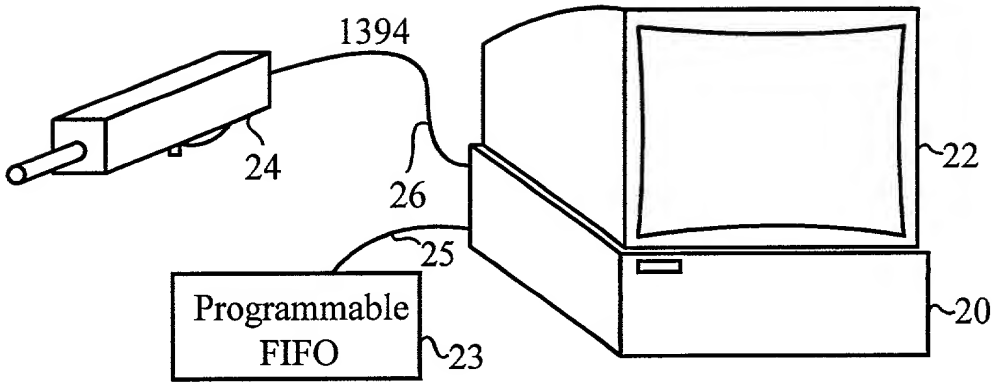


Fig. 4

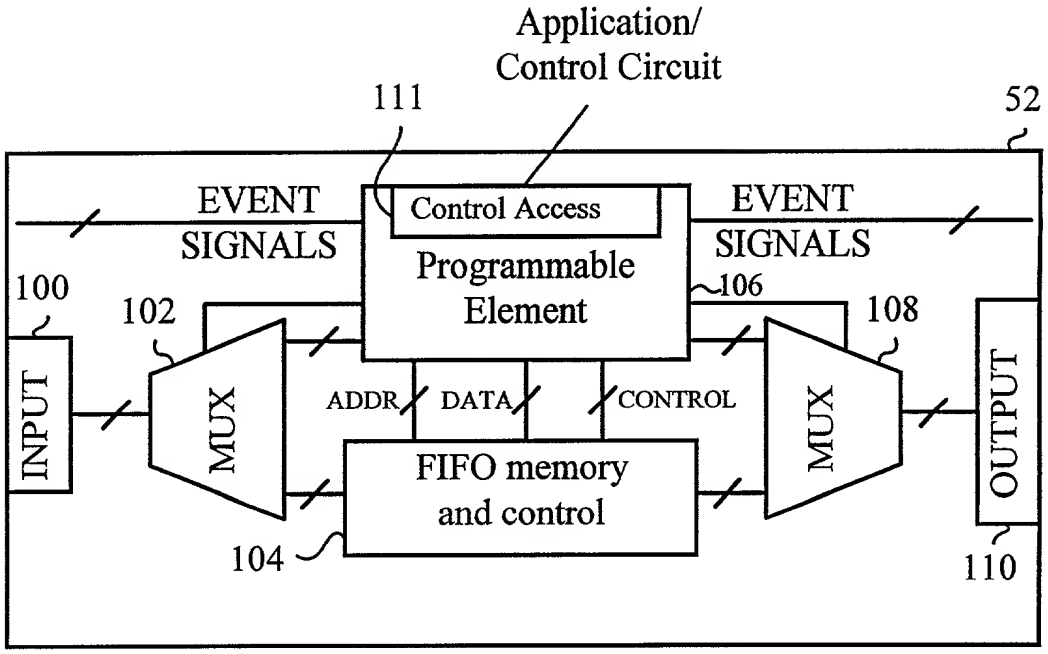

Application/
Control Circuit
111
52
EVENT
SIGNALS
Control Access
Programmable
Element
EVENT
SIGNALS
100
102
106
108
INPUT
MUX
ADDR
DATA
CONTROL
MUX
OUTPUT
FIFO memory
and control
104
110

Fig. 5

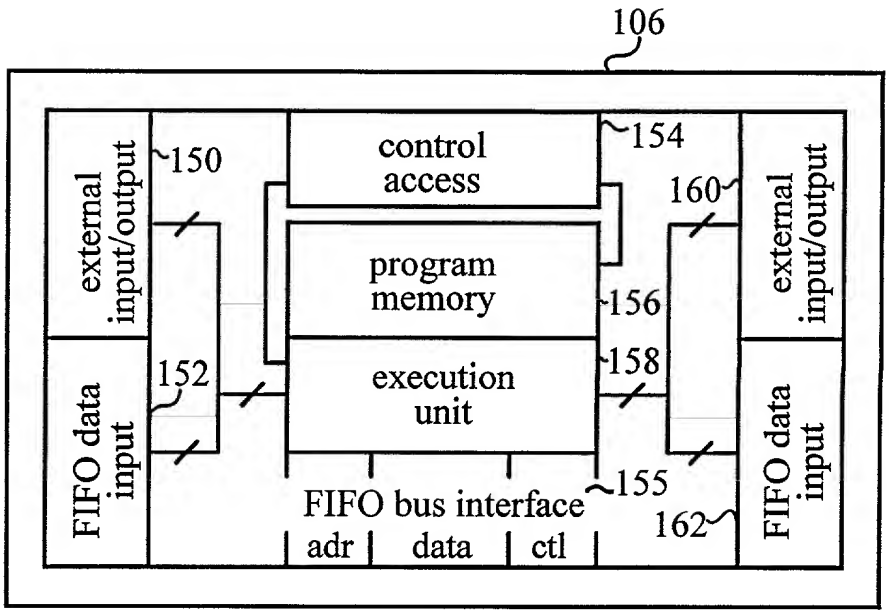
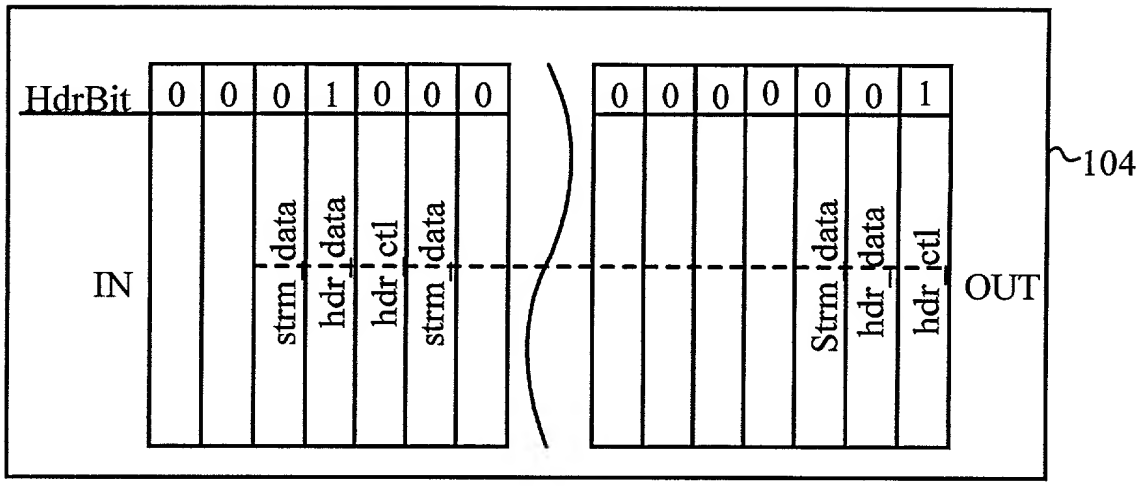

106
external input/output
150
control access
154
160
program memory
156
external input/output
FIFO data input
152
execution unit
158
FIFO data input
FIFO bus interface
155
162
adr
data
ctl

Fig. 6



FIFO Contents

Fig. 7

EXPRESS MAIL LABEL #EL703161567US

PATENT

Attorney Docket No.: SONY-14500

COMBINED DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY

As a below-named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name. I believe I am an original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: **PROGRAMMABLE FIRST-IN FIRST-OUT (FIFO) MEMORY BUFFER FOR CONCURRENT DATA STREAM HANDLING**. The specification of which is attached hereto. I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claim	
			Yes	No
Number	Country	Day/Month/Year Filed		

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below

Application Serial No.	Filing Date

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application Serial No.	Filing Date	Status: Patented, Pending, Abandoned

I hereby appoint the following as my attorneys with full power of substitution to prosecute this application and transact all business in the Patent and Trademark Office in connection therewith:

Thomas B. Haverstock	32,571	Jonathan O. Owens	37,902

Please direct all correspondence regarding this application to the following:

Jonathan O. Owens
HAVERSTOCK & OWENS LLP
260 Sheridan Avenue, Suite 420
Palo Alto, California 94306

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of First Sole Inventor: Bruce A. Fairman

Inventor's Signature: Bruce A Fairman 2 NOV 00
Date

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